CLAIMS

1. A system comprising:
shared system registers, each register including an access protocol and data; and
N processors, $N \geq 2$, where N is an integer, each accessing the registers.

2. A system, as defined in claim 1, the access protocol including a configurable access type for each N processors.

3. A system, as defined in claim 2, the access type being selected from a group that includes READ, READ/CLEAR, READ/SET, and READ/WRITE.

4. A system as defined in claim 3, comprising programmable configuration registers operative to encode and store the access protocol, each configuration register corresponding to one of the shared system registers.

5. A system, as defined in claim 4, wherein:
each programmable configuration register consisting of N*2 bits; and
the configurable access types are encoded into 2 bits.

6. A system as defined in claim 3, the access protocol encoded and provided as input signals to the hardware design.

7. A system, as defined in claim 3, the access protocol encoded and selected as a build-time option in the hardware design source code.

8. A system, as defined in claim 3, the access protocol further including an arbitration priority.

9. A system as defined in claim 8, comprising programmable configuration registers operative to encode and store the access protocol, each configuration register corresponding to one of the shared system registers.

10. A system, as defined in claim 9, wherein:

N is 2; and

each programmable register including 5-bits, 2 bits represent the access type of one of the two processors, 2 bits represent the access type of the other of the two processors, and 1 bit represents the arbitration priority.

11. A system, as defined in claim 9, wherein:

each programmable configuration registers consists of $N*(2 + \text{ceiling}(\log_2 N))$ bits; and

the access protocol including the four access types are encoded into 2 bits per processor and the arbitration priority encoded into $\text{ceiling}(\log_2 N)$ bits.

12. A system, as defined in claim 8, the access protocol encoded and selected as a build-time option in the hardware design source code.

13. A system as defined in claim 8, the access protocol encoded and provided as input signals to the hardware design.